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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/634,242	08/05/2003	Harry Hedler	1406/158	6396
25297 7	590 09/09/2004		EXAMINER	
JENKINS & WILSON, PA			CLARK, SHEILA V	
3100 TOWER BLVD SUITE 1400		ART UNIT	PAPER NUMBER	
DURHAM, NC 27707			2815	
		DATE MAILED: 09/09/2004		

Please find below and/or attached an Office communication concerning this application or proceeding.

	Application No.	Applicant(s)				
Office Action Summers	10/634,242	HEDLER ET AL.				
Office Action Summary	Examiner	Art Unit				
	S. V. Clark	2815				
The MAILING DATE of this communication appears on the cover sheet with the correspondence address Period for Reply						
A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.  - Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.  - If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.  - If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.  - Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).  Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).						
Status						
1) Responsive to communication(s) filed on	_•					
2a) ☐ This action is <b>FINAL</b> . 2b) ☑ This						
)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the ments is						
closed in accordance with the practice under Ex parte Quayle, 1935 C.D. 11, 453 O.G. 213.						
Disposition of Claims						
4)⊠ Claim(s) <u>1-20</u> is/are pending in the application.						
4a) Of the above claim(s) is/are withdrawn from consideration.						
5) Claim(s) is/are allowed.						
6)⊠ Claim(s) <u>1-10 and 14-19</u> is/are rejected.	6)⊠ Claim(s) <u>1-10 and 14-19</u> is/are rejected.					
7) Claim(s) <u>11, 12-13, 20</u> is/are objected to.	☑ Claim(s) <u>11, 12-13, 20</u> is/are objected to.					
8) Claim(s) are subject to restriction and/or	r election requirement.					
Application Papers						
9)☐ The specification is objected to by the Examine	r.					
10) The drawing(s) filed on is/are: a) acce	epted or b) $\square$ objected to by the $\mathfrak l$	Examiner.				
	Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).					
	Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).					
11)☐ The oath or declaration is objected to by the Ex	aminer. Note the attached Office	Action or form PTO-152.				
Priority under 35 U.S.C. § 119						
12)⊠ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  a)⊠ All b)□ Some * c)□ None of:						
1.⊠ Certified copies of the priority documents have been received.						
2. Certified copies of the priority documents have been received in Application No						
3. Copies of the certified copies of the priority documents have been received in this National Stage						
application from the International Bureau (PCT Rule 17.2(a)).						
* See the attached detailed Office action for a list of the certified copies not received.						
Attachment(s)						
1) Notice of References Cited (PTO-892)  4) Interview Summary (PTO-413)  Paper No(s)/Mail Date						
2) Notice of Dransperson's Patent Drawing Review (P10-946)  3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  Paper No(s)/Mail Date 2000 00000000000000000000000000000000		Patent Application (PTO-152)				
7/11						

Application/Control Number: 10/634,242

Art Unit: 2815

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Claims 1-20 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. It is unclear what if meant by, the structure whereby the solder layer assumes the structure of the interconnect level. The solder layer depicted in the drawings and described in the specification fails to have a structure like the interconnect level. The solder layer is rounded and appears to have a greater thickness than the interconnect base levels. What is meant by "assuming the structure"? Clarity is suggested.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

Claims 1-4, 5-9, 10, 15-18 insofar as definite are rejected under 35 U.S.C. 102(a) as being anticipated by Boettcher.

Boettcher et al teaches applying a interconnect level 4, 5 to a semiconductor substrate 1 and structuring said level and applying a solder layer 16 on the interconnect level. Use of photolithographic techniques is taught in col. 5, line 41 and sputter deposition is taught in col. 5, line 36 and the metals recited in the claims are taught in col. 5, lines 27-28, 61-63. The solder layer formed by reflow soldering is taught in col. 2, line 4. and dip soldering is taught in col. 2, line 41

(plating bath discussion). Figure 2F shows solder 16 formed over the sidewalls of interconnect 10.

The structure recited in claims 15-18 has been discussed above.

Claims 1, 8, 10, 14 insofar as definite are rejected under 35 U.S.C. 102(a) as being anticipated by Homma et al

Homma et al teaches applying a interconnect level 4, 5,6 to a semiconductor substrate 1 and structuring said level and applying a solder layer 10 on the interconnect level and use of solder resist 8 before application of solder 10- ( see col. 20-44). The structure recited in claim 10 is taught in figure 24. Use of palladium in the interconnect is taught in col. 7, line 13.

Claims 1-10, 14, 15-19 are rejected.

Claims 11, 12-13, 20 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Any inquiry concerning this communication should be directed to S. V. Clark at telephone number (571) 272-1725.

> Primary Examiner Art Unit 2815

Page 3

September 6, 2004